# SOLDER JOINT RELIABILITY ON MIXED SAC-BISN BALL GRID ARRAY SOLDER JOINTS FORMED WITH RESIN REINFORCED BI-SN METALLURGY SOLDER PASTES

Olivia H Chen<sup>1</sup>, James Gao<sup>4</sup>, Tim C.C. Pan<sup>4</sup>, Kok Kwan Tang<sup>3</sup>, Raiyo Aspandiar, Ph.D.<sup>2</sup>, Kevin Byrd<sup>2</sup>, Bite Zhou<sup>2</sup>, Scott Mokler<sup>2</sup>, and Al Molina<sup>1</sup>

<sup>1</sup>Intel Corporation, Folsom, CA, USA
 <sup>2</sup> Intel Corporation Hillsboro, OR, USA
 <sup>3</sup>Intel Corporation Kulim, Malaysia
 <sup>4</sup>Wistron InfoComm (Kunshan) Co., Ltd., Kunshan, PRC olivia.h.chen@intel.com

### ABSTRACT

Due to the decreasing size of consumer electronic products such as smart phones, tablets, and personal computers, ultrathin flip chip ball grid array (FCBGA) packages are needed to meet the demand of lower z-heights for slimmer form factors. However, packages used in consumer electronics are commonly assembled on printed circuit boards (PCB) with lead-free SnAgCu (SAC) solder paste at peak reflow temperatures in the 240C to 260C range. Assembly challenges are observed at these peak reflow temperatures due to dynamic warpage of the component substrates of ultra-thin FCBGAs, as well as the PCB. The Bi-Sn low temperature solder metallurgical system has been proposed as an alternative to the SAC metallurgical system to overcome these package substrate and PCB warpage induced assembly challenges. Besides improving solder joint yields on ultra-thin FCBGAs, the lower melting point of this Bi-Sn metallurgy also enables manufacturing cost savings and environmental benefits.

However, based on previous literature studies, the presence of Bi in Sn-based low temperature solder has exhibited solder joint embrittlement and thereby decreased the mechanical shock resistance of such solder joints. In order to strengthen the solder joint, low temperture solder pastes have been developed containing resin, which by flowing around the solder joint and curing during the reflow process it provides polymeric encapsulation reinforcement at the solder joint level. In a previous study [16], this type of low temperature joint reinforced paste (JRP) had shown improved mechanical shock resistance on mixed BiSn+SnAgCu FCBGA solder joints when compared to those without the polymeric encapsulation. However, the effect of thermal fatigue on the resin reinfroced BiSn+SnAgCu BGA solder joint when subjected to thermal cycling needed to be better understood.

In this paper, the investigation centered on both the mechanical shock and the thermal cycling performance of the mixed BiSnAg (BSA)+SAC solder joints assembled with JRP pastes on a Flip Chip Molded Package BGA (FCMB) and compared the data to those assembled with

SAC305 paste. Reliability failure rate characterized with Weibull distributions, failure modes and locations within the solder joint stack-up were determined. Results indicated that the mixed SAC+BiSn solder joints with polymeric reinforcement when using two different JRPs were less shock resistant than the SAC solder joints for both JRPs. More development is therfore necessary with JRPs to enable low temperature Bi-Sn solder joints to become comparable with un-reinforced SAC BGA solder joints under mechanical shock. There was significant improvement in the thermal cycling performance for mixed SAC+BiSn solder joints formed using one of the JRPs, but this improvement was for the solder joints located at the package corners only. The level of encapsulation of the solder joints by the reinforcing resin was inconsistent across the FCMB array and this could have caused this inconsistent temperature cycling resistance.

Key words: BGA solder joints, low temperature solder, Bi-Sn metallurgy, Mechanical Shock Reliability, Temperature Cycle Reliability, Polymeric reinforcement

### INTRODUCTION

Original Design Manufacturers (ODMs) have a perpetual motivation to reduce their manufacturing costs and through put time (TPT) for enhancing their financial margins. This has driven some ODMs in the Far East to explore the use of low temperature solders as a replacement for the lead-free SAC solders in consumer electronic products, such as cell phones, tablets and mobile computers.

Low temperature solders have a number of benefits from an ODM perspective. There are economic benefits related to the reduced power costs [1,2,3] in operating solder equipment such as reflow ovens and the potential use of cheaper components and boards due to the elimination of the need for components and boards to survive high SAC reflow temperatures [4]. Associated with the reduced power costs is the environmental benefit of a reduced carbon footprint [1].

Low temperature solders also have an assembly yield improvement benefit. This is related to the reduced warpage of thinner packages at the lower peak reflow temperatures [1,2,4]. Excessive warpage of components such as BGAs causes specific solder defects such as Head-on-Pillow (HoP), Non-Wet Opens (NWO) and solder bridging [5,6,7]. Increasing yield will indirectly reduce manufacturing cost by reducing or eliminating the need to rework and/or scrap electronic assemblies.

The low temperature metallurgy system of choice at present is the Bi-Sn system. The Bi-Sn eutectic (57 wt% Bi) has a melting temperature of 138C [8]. Beyond its lower melting temperature, this Bi-Sn solder system has other benefits. Bi-Sn solders are presently being used in low cost consumer electronics products, such as CD players, TVs, and kitchen appliances, and therefore there is already some assembly process experience of Bi-Sn solders within the ODMs. The typical peak reflow temperature ranges of the Bi-Sn solders is 160 to 190C. The dynamic warpage characteristics of most FCBGA components, results in their warpage being near zero, since the 'inversion temperature', which is the temperature at which FCBGAs invert from a concave ( smile) shape to a convex ( frown) shape, falls within this range. This characteristic enables the soldering of FCBGAs with SAC balls using the Bi-Sn solder paste at high yields without the complete melting and collapse of the SAC solder ball [1,2].

However, the Bi-Sn metallurgy system as a solder material has a major drawback. The Bi-Sn solders are brittle [9] particularly at high strain rates [10]. The inherent brittle nature of bismuth, is largely attributed to its rhombohedral crystal structure [11], which has very few of the slip planes that are necessary for material ductility. In fact, bismuth has only 1/3 the slip planes found in Sn and 1/6 the slip planes found in Cu, Ni, Al and Pb [12]. The brittleness of Bi-Sn based solder alloys can limit their use in cell phones, tablets and other mobile devices, which can be subjected to multiple drops during use. Mixed Alloy BGA solder joints formed by soldering SAC solder balls with BSA solder paste have been shown to exhibit significant reduction in mechanical drop reliability when compared with solder joints formed using SAC based solder pastes [13,14,15]. This reduced drop resistance is caused by the bismuth presence in the solder joint stiffening the solder and making the intermetallic compound (IMC) at the solder-to-land interface more brittle.

In the quest to overcome this drawback, two avenues have been pursued. One is to modify the metallurgy of the BiSn alloy to make it less brittle. This is being done by reducing the bismuth content, micro-alloying the solder with other elements to impart grain refinements and precipitate strengthen the alloy. A companion paper by Mokler, et.al., [2] describes this effort in more detail.

A second way is to use polymers to locally encapsulate the solder joints partially and thereby reinforcing them to

survive the forces during a mechanical shock event. This is being done by the use of Joint Reinforcement Pastes (JRP). The polymer resin is incorporated within the solder paste. The resin gels and cures during the reflow soldering process. But, this gelling and curing takes place after the Bi-Sn solder has melted, wetted the surfaces to be adhered, and forced the resin to the perimeter of the joint.

A previous paper by the authors [1] focused on the solder paste printability, reflow profile comparison and SMT solder joint yield when using standard BSA and resin reinforced solder pastes. Two other papers by the authors [16, 17] presented preliminary shock results on FCBGA solder joints using one JRP. This paper will continue the evaluation of mechanical shock resistance of polymerically reinforced mixed SAC-BSA BGA solder joints. But, in this case, (i) another JRP from a different manufacturer will also be evaluated, and (ii) the component used here is a Flip Chip Molded Package BGA (FCMB) with a memory package on top.

### EXPERIMENTAL

Various aspects of the experimental strategy in this study are expounded below.

### Package Test Vehicles

Since FCBGA packages had been evaluated before, the FCMB package was chosen for evaluation. Figure 1 depicts the top, bottom and side views of the FCMB package. Table 1 and 2 list the various attributes shown in Figure 1.

A JEDEC standard memory package was mounted on the top of the FCMB4 package during surface mount assembly to form a Package-on-Package (PoP) structure. This memory package had a 14x14mm body size, with 220 balls at 0.5mm pitch.

### Printed Circuit Board Test Vehicle

The printed circuit board test vehicle for shock testing was designed in accordance to JEDEC JES022-B111 specification which is a widely used industry standard to assess mobile product drop use conditions. The test board, which is shown in Figure 2, had dimensions of 132mm x 77mm x 1mm with 8 layers design. The board contained (15) FCMB components with 10mil metal defined (MD) land patterns and 13mil round solder resist opening (SRO) and an organic solderability preservative (OSP) surface finish.

There were a total of four monitoring daisy chain nets on each component. The location of the daisy chains are shown in Figure 3. Daisy chain nets from each of the components patterns were brought out to a card edge connector and soldered connections were used to monitor the resistances of the daisy chain nets during drop and temp cycle testing.

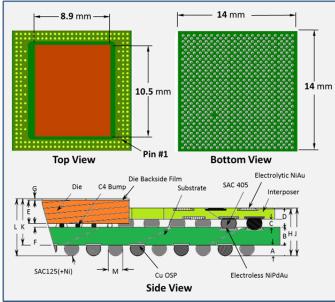


Figure 1. Detailed Top, Bottom and Side Views of the FCMB package

Item	Attribute	Dimension (mm)
Α	BGA Balls Attached	0.116
В	Substrate Thickness	0.262
Е	Die Thickness	0.270
F	Die Gap Height	0.055
G	Die Backside Film (DBF)	0.020
J	Interposer Height (pre-SMT)	0.605
Н	Substrate ball to Interposer Top Metal Plate	0.594
К	Substrate Ball to Interposer Solder Resist Top	0.605
L	Bottom of Substrate to Top of DBF	0.611
М	Bottom of ball to Top of DBF	0727

Table 1. Attributes for the FCMB package in Figure 1

Table 2. Attributes for Substrate and Interposer in Figure	Table 2.	Attributes	for	Substrate	and	Interposer	' in	Figure
--	----------	------------	-----	-----------	-----	------------	------	--------

Item	Attribute	Тор	Bottom
	Solder Resist Opening (mm)	0.25	0.28
trate	Ball Pitch (mm)	0.4	0.483
Substrate	Pre-Attach Solder Ball (mm)	n/a	0.203
•1	Ball Count	276	760
	Solder Resist Opening (mm)	0.28	0.25
poser	Ball Pitch (mm)	0.5	0.4
Interposer	Pre-Attach Solder Ball (mm)	n/a	0.254
Ι	Ball Count	220	276

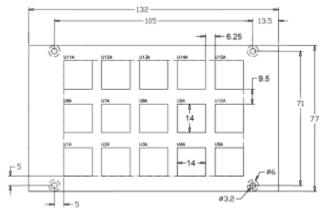


Figure 2. JEDEC Test Board Size and Layout

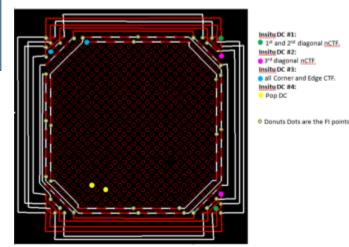


Figure 3. Daisy Chain Coverage of the Monitoring FCMB4 Component

#### **Experimental Design**

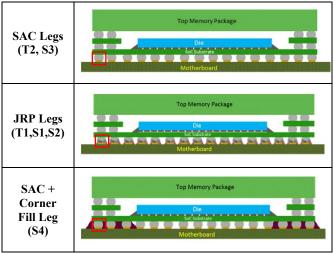
There are three main variables for the experimental design. The type of reliability test (mechanical shock and temperature cycling), the solder paste used (SAC 305 and two different JRPs) and the presence or absence of corner fill adhesive under the package. The Experimental Design Matrix is given in Table 3. The sample sizes for each leg are also listed in the table.

The two specific reliability tests were chosen since these are the two primary reliability tests that are required for all Intel package platforms. SAC305 solder paste was used for the control legs, and two different JRPs were used for comparison. One leg with corner fill was added since presently some BGA components on product boards have corner fill adhesives applied after reflow soldering. This leg was tested under mechanical shock only since the corner fill is used to impart shock resistance rather than to improve temperature cycling fatigue life. If JRP solder joints met the shock and temp cycle requirements, the corner fill step in thereby production could be eliminated saving manufacturing costs and increased TPT.

Table 3. Experimental Design Matrix

Leg	Reliability	Solder	Corner	Sample Size	
#	Test	Paste	Fill	Boards	Cmpnts
T1	Temp	JRP1	No	2	30
T2	Cycle	SAC305	No	1	15
S1		JRP1	No	6	24
S2	Mechanical	JRP2	No	6	24
S3	Shock	SAC305	No	5	20
S4		SAC305	Yes	3	12

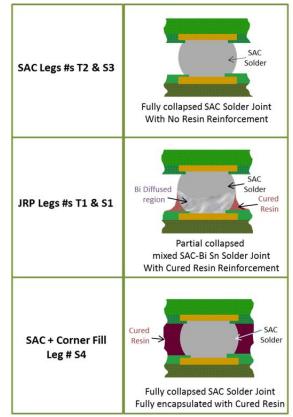
The FCMB area array solder joint make up after reflow soldering would vary for each of the legs depicted in Table 3. Figure 4 shows a cross-sectional diagram of the FCMB POP assembly for each of the legs in Table 3. Figure 5 shows detail of an individual solder joint in the corner region of the FCMB package array, as identified by the small squares in Figure 4.



**Figure 4.** Cross-sectional Diagrams of the FCMB POP Assembly for the experimental legs evaluated.

### **Assembly Process**

Solder Paste was printed on the lands of all test sample boards using a 100 microns thick stainless steel, laser-etched, electro-polished stencil. A variable aperture design was used for this stencil. This design is depicted in Figure 6 which gives the aperture for each land in the FCMB package area array. The outer row had a square shape with 305 microns per side. The next two inner rows also had a square shape but with slightly smaller side of 280 microns. The rest of the pads in the inner section of the array were circular with a diameter of 280 microns. More paste was printed on the outer lands to account for the `smiley face` warpage of the FCMB package at the SAC reflow temperatures.



**Figure 5.** Single Joint Cross-sectional Diagrams of the FCMB PoP for the experimental legs evaluated

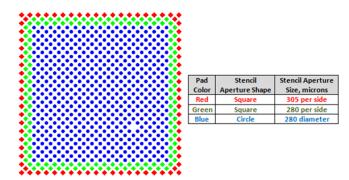


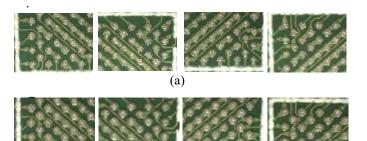
Figure 6. Stencil design of BGA Test Vehicle paste print

The print tool parameter settings used are listed in Table 4. These print tool parameter settings had previously been optimized for the SAC305 POR paste and these same settings were used for the two JRP low temperature solder pastes. Despite this lack of optimization in the print settings for the JRPs, their print results did not show solder bridging or missing solder. Figure 7(a) and 7 (b) shows photos of a few prints with both JRP1 and JRP2 pastes, respectively. The solder paste volume transfer efficiency were similar for both JRP1 (~90.1%) and JRP2 (~84.4%), as shown in Figure 8.

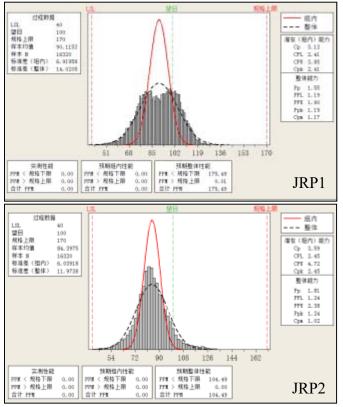
**Table 4.** Solder printing parameters tuned for printing SAC,

 JRP1 and JRP2 pastes

ord r and ord 2 publics		
Squeegee angle	60 degrees	
Print speed	100mm/s	
Printing pressure	10kg	
Separation speed	1.0mm/s	
Separation distance	3.0mm	



(b) **Figure 7.** Solder printing result for (a) JRP 1 and (b) JRP 2



**Figure 8.** Solder paste volume transfer performance for round aperture for both JRP1 and JRP2

Reflow soldering was done in an Air ambient, without a pallet, using reflow profiles developed to match the solder paste supplier recommendations. These reflow profiles are shown in Figures 9, 10 and11), for the JRP1, JRP2 and SAC305 solder pastes, respectively.

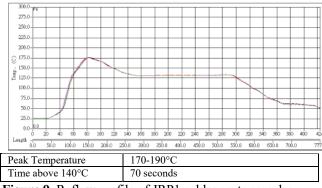


Figure 9. Reflow profile of JRP1 solder paste samples

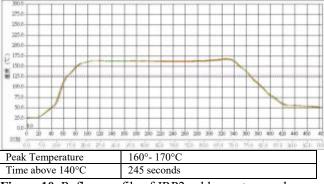


Figure 10. Reflow profile of JRP2 solder paste samples

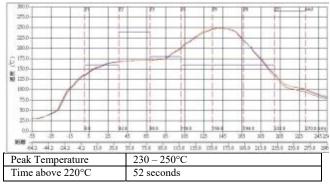


Figure 11. Reflow profile of SAC solder paste samples

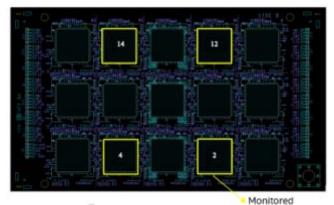
### **Mechanical Shock Test Protocol**

The following mechanical shock and temp cycle test conditions were used to assess the FCMB packages assembled with low temperature JRP solder and SAC305 solder paste.

Samples for shock testing were subjected to 1500G, 0.5ms, half-sine pulse based on JES022-B111 [18] for forty drops in the top down orientation, as listed in Table 5.

Table 5. Shock Test	s. SAC DOE		
Input	Level	#of drops	Orientation
Half Sine shock pulse Pulse duration	1500 g's, +/- 10% 0.5ms	40	Top Down

Though each board test vehicle sample had 15 total FCMB PoP components mounted on it, only 4 components were monitored for solder joint failures during the shock test. The location of these 4 components is shown in Figure12. These components were monitored electrically (in-situ) during the duration of the test using the daisy chain design shown in Figure 3. The daisy chain designators are shown in Figure 13.



**Figure 12.** Components Monitored in-situ during Shock Testing (four components/board)



1<sup>st</sup> and 2<sup>nd</sup> row NCTF 3<sup>rd</sup> row NCTF Common GND Corner and Edge CTF PoP DC (Not Monitored in

**Figure 13.** Daisy chain net designators for Shock and Temp cycle coverage. NCTF = Non critical to function; GND = Ground; CTF = Critical to function

Shock)

The shock test samples were setup with the board placed in a fixture in the top down orientation on a High-G shock table. This setup is shown in Figure 14.

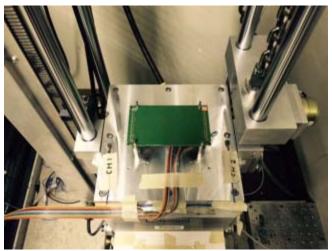


Figure 14. Shock Test Setup

## **Temperature Cycling Test Protocol**

The temperature cycling test profile is shown in Figure 15. It entailed dwell temperatures of -40C and 100C, with a 15min soak at each dwell temperature and a, 10C/min ramp between the dwell temperatures. The total cycle time was 50min/cycle. Temp cycle data collection was carried out per IPC 9701A specification [19]

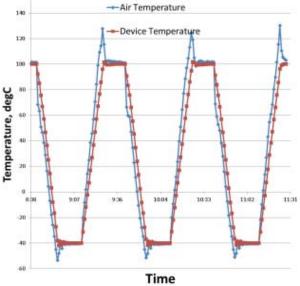


Figure 15. Temp Cycle Test Profile

A single zone thermal cycle chamber was used with the boards seated vertically in card cages during the test to ensure minimal airflow obstruction. All 15 assembled FCMB PoP components on the test board were monitored for solder joint failures. These 15 locations are shown in Figure 16.

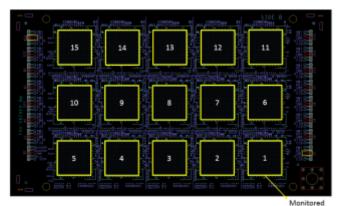


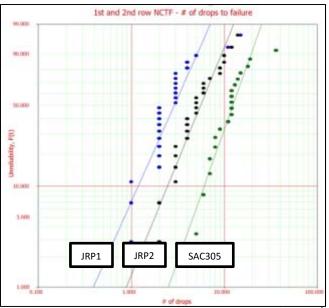
Figure 16: Components monitored in-situ during Temp Cycle testing

## **RESULTS AND DISCUSSION In-situ Shock Test Results**

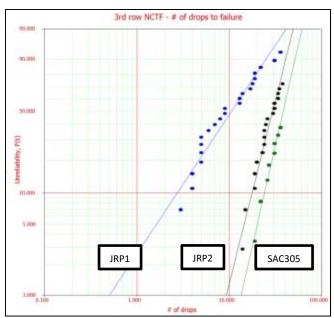
The 1<sup>st</sup> and 2<sup>nd</sup> row NCTF daisy chain nets located in the package corners (AW1 net in Figure 13) were the first nets to show failure on both SAC and JRP legs. The 3<sup>rd</sup> Row NCTF daisy chain net (AR1 in Figure 13) was the next to show failures on both SAC and JRP legs. The CTF daisy

chain net (AT38 in Figure 13) was the last to show failure for the JRP legs but did not show any failures for the SAC leg. As expected, the SAC+ corner fill leg (#S4 in Table 3) did not show any failures.

The 2-P Weibull distribution data plots for the 1<sup>st</sup> and 2<sup>nd</sup> row NCTF, the 3<sup>rd</sup> row NCTF and the CTF daisy chain nets are shown in Figures 17, 18 and 19, respectively. Table 6 lists these results in terms of the characteristics lives of the data, i.e., number of drops for 63.2% failure rate. Performance of the resin reinforced mixed SAC-BiSn solder joints is still not comparable to standard SAC solder joints or SAC solder joint with corner fill. The margin loss is as much as 78% when comparing characteristic lives.



**Figure 17.** Weibull 2-P distribution of Net AW1 (1<sup>st</sup> and 2<sup>nd</sup> row NCTF) comparing JRP1, JRP2, and SAC305



**Figure 18.** Weibull 2-P distribution of Net AR1 (3<sup>rd</sup> row NCTF) comparing JRP1, JRP2, and SAC305

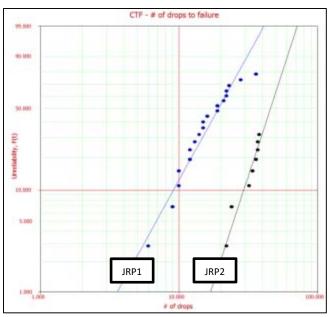


Figure 19. Weibull 2-P distribution of CTF net comparing JRP1 and JRP2

<b>Table 6.</b> Shock Characteristic life comparison between	
SAC305 (POR), JRP 1, JRP2 and SAC305 + Corner Fill	

DOE	Characteristic Life (# of drops to 63.2% failure)				
DOE	1 <sup>st</sup> & 2 <sup>nd</sup> NCTF	3 <sup>rd</sup> NCTF	CTF		
JRP1	3	14	22		
JRP2	7	33	50		
SAC305	14	42	No Fail		
SAC+C. Fill	No fail	No Fail	No Fail		

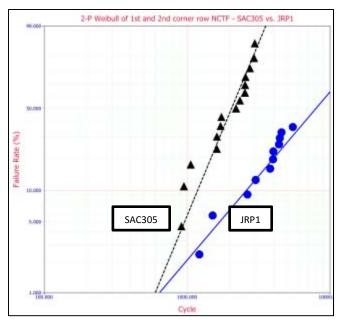
Additionally, the data points out that the JRP2 leg showed better shock performance than JRP1 leg. This can possible be attributed to two factors. First, the resin from JRP1 is stiffer than JRP2, based on supplier documented room temperature modulus values of the cured resin (14.0 GPA for JRP1 and 3.2 GPA for JRP2). Second, the level of encapsulation by the cured resin of the solder joints with JRP2 is higher than that for JRP1 since the metal content of JRP1 (85%) is more than that for JRP2 (82%). The cohesive strength of the two resins as well as their adhesion to both the solder joint and the solder mask on the board also play a part in their shock response, but these values are not known at this time.

These results highlight that there is additional work needed to strengthen the FCMB mixed SAC-BiSn solder joints for the use of low temp solder in small form factor mobile application.

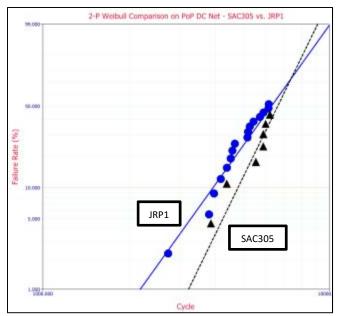
### In-situ Temperature Cycle Test Results

The temperature cycle test was carried out to 6500 cycles when 80% of the samples had reached failure on both the JRP1 and SAC305 legs on the first two monitored daisy chain nets. As pointed out in Table 3, there were only two legs for the temperature cycling part of this study due to limitations in the availability of package test vehicles.

Among the monitoring nets, the package corners and two PoP DC pins closer to the inner row region of the package were the first to show failures. A 2-P Weibull distribution using Maximum Likelihood (MLE) method was used to analyze the in-situ data collected per IPC9701A methodology [19]. From the Weibull distribution shown in Figure 20 and 21, and Table 7, which lists the characteristic life for both legs, the JRP1 leg showed better reliability margin than SAC305 by ~300% at the AW1 location (corner most 1<sup>st</sup> and 2<sup>nd</sup> row) based on characteristic life comparison. However, on the two PoP DC pins, JRP1 showed almost comparable, with only 2% lower, characteristic life to SAC305.



**Figure 20.** Weibull 2-P distribution of JRP1 vs. SAC305 on AW1 (1<sup>st</sup> and 2<sup>nd</sup> row NCTF)



**Figure 21**. Weibull 2-P distribution of JRP1 vs. SAC305 on F26 (PoP DC at inner package region)

The in-situ Weibull results showed that the reliability of JRP1 can be package location dependent, which can result from the variation in resin encapsulation coverage from the package inner row region to the package corner. In addition to using resin reinforcement to add shock margin, the resin encapsulation amount surrounding the solder joint can play an important role on thermal cycle fatigue failure. More will be discussed in the failure analysis section in this paper as we compare the encapsulation percentage at various package locations.

**Table 7.** Characteristic life comparison between JRP1 and SAC305 on 1<sup>st</sup> and 2<sup>nd</sup> NCTF and PoP DC

DOE	Characteristic Life (# of cyc to 63.2% failure)			
	1 <sup>st</sup> & 2 <sup>nd</sup> NCTF	F26 PoP DC		
JRP1	9907	6876		
SAC305	2275	7023		

### **Failure Analysis on Mechanical Shock Samples**

The post shock test dye and pull failure analysis results confirmed the failure trend from in-situ shock data. Figure 22 shows the various possible failure disbond interfaces after the package has been pulled from the board. Figure 23 displays the Dye and Pull Maps on the failure distribution within the FCMB package solder joint array. More dye penetration and solder joint cracks were observed in JRP legs compared to SAC305. Due to metallurgy differences from Bi segregation, JRP legs (Bi-Sn based) both showed dominant Type 3 disbond type, where solder joint cracks formed between PCB pads and solder joint IMC at the brittle interface. SAC305's dominant disbond mode is Type 4, between the PCB pad and PCB laminate which is sometimes termed 'pad cratering'. Table 8 summarized the data from Figure 23. Both JRP legs show a larger number of cracked joints compared to SAC305. Also, a larger number of cracked joints with similar % of dyed area were found on JRP1 compared to JRP2, which is consistent with the in-situ failure data.

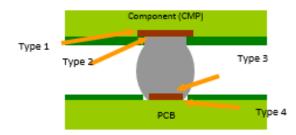


Figure 22. Failure disbond type categories

Cross sectioning was done on some failed samples for both JRP1 and JRP2 to confirm resin coverage as well as failure disbond location. Most failures occurred at the Type 3 interface (in the bulk solder near the Bi rich region), which is consistent with what was found in the Dye and Pull results. SAC and SAC+Corner fill legs cross sections were also done on passing samples to check corner fill coverage and overall joint formation. The cross section cuts were made along the edge most rows, where shock failure first occurred, to inspect epoxy coverage on corner joints of the JRP legs. Both JRP1 and JRP2 joints showed partial and full resin encapsulation along the location of interest, as shown in Figure 24. Figure 25 and 26 show cross-section examples for the SAC leg and the SAC+Corner Fill leg, respectively.



**Figure 23.** Post shock test Dye and Pull failure distribution map for FCMB package solder joint array. Left – JRP1, Center JRP2, Right SAC305. The coloring and number represents the frequency of large crack occurrence. 10 =high; 1 = low

<b>Table 8.</b> Summary table showing JRP and SAC305 crack
disbond type and dye penetration percentage



**Figure 24.** Cross section on JRP1 and JRP2 showing corner and edge encapsulation. Green arrow: Full coverage; Pink: Partial coverage

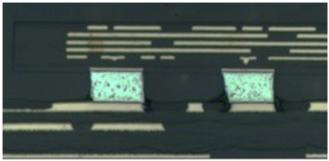


Figure 25. Cross Section of SAC305 joint

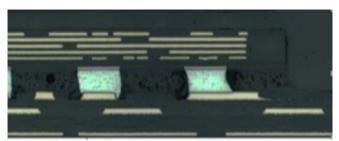
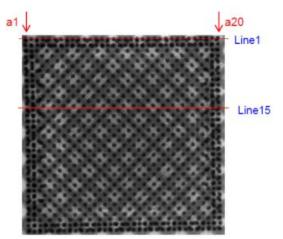


Figure 26. Cross Section of SAC305+Corner fill to show corner fill coverage.

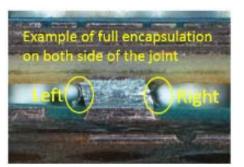
### Failure Analysis on Temp Cycle Samples

Cross sections were done immediately after reflow soldering (i.e., pre temperature cycling) on package locations shown in Figure 27 to determine the extent of resin encapsulation height on the solder joints. Higher encapsulation height was found on corner/edge package location compared to package center, as seen in Figure 28. The package edge row also showed a total of seven joints with full resin encapsulation on both the left and right sides of the solder joint, as seen in Figure 29. Areas with more resin coverage improved the temperature cycling reliability. This variation in resin coverage also lead to the temp cycle characteristic life margin differences observed on JRP1 and SAC305 at 1<sup>st</sup> and 2<sup>nd</sup> NCTF and F26 DC POP nets. More details will be discussed in the section below.

In addition to pre-temperature cycling cross sections, dye and pull as well as end of test cross section were also done on selected units after thermal cycle test reached 6500cyc. The cross section cuts' location is shown in Fig. 30.



**Figure 27.** Pre-Temp Cycle, cross section location on two package location. Line1 = Edge coverage; Line15 = Closer to package die shadow region



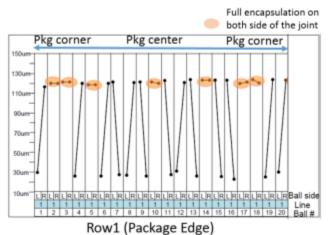


Figure 28. Pre Temp Cycle, resin coverage variation on solder joints in the Package Edge row

Figure 31 shows the crack propagation in SAC305 joints at the end of test. Most cracks occurred in the bulk solder, at a mix of type 2 and type 3 interfaces. Compared to SAC305 legs, the JRP leg showed crack propagation mostly at the type 3 interface which is in the Bi rich region, as seen in Figure 32. The Bi diffusion led to localized stress concentration points in the Bi region, which can potentially lead to higher thermal fatigue stress.

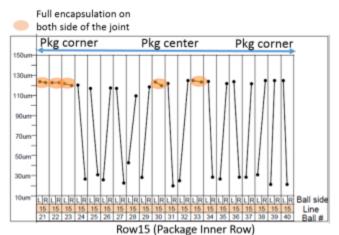
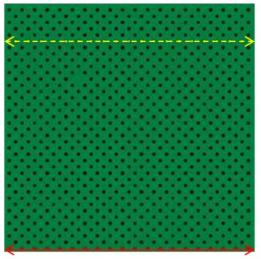


Figure 29. Pre-temp cycling resin coverage variation of solder joints in the Package Inner Row



**Figure 30.** Post temp cycle test sample cross section locations. Red Full line = Edge row (AW1 net); Yellow dashed line = Package die shadow (F26 net)

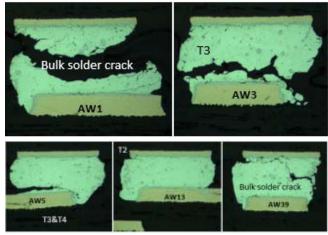


Figure 31. Post temp cycle test cross section on edge row for SAC305 leg

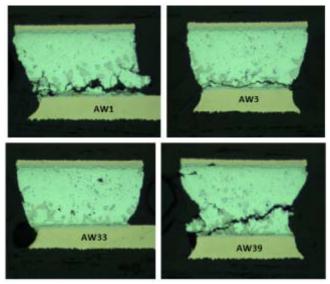


Figure 32. Post Temp Cycle Cross-sections of solder joints on the edge row for the JRP1 leg

Figure 33 shows post temp cycle cross sections for the JRP1 leg. The variation of resin encapsulation of the edge row, which has mostly full coverage, versus the inner row which are mostly fillet coverage is easily apparent. This is consistent with the observations made when inspecting the pre-temp cycle cross-sections in Figure 28. The coverage variation between inner row and package edge can also be the key to the margin difference on JRP1 vs. SAC305 temp cycle reliability of the two monitoring nets. The corner 1<sup>st</sup> and 2<sup>nd</sup> row NCTF net with more joint encapsulation showed significantly better temp cycle reliability margin than SAC305, while inner row F26 PoP net with fillet coverage only showed comparable performance to SAC305.

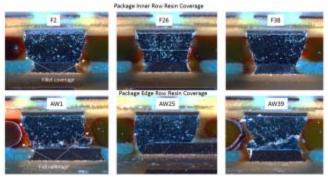
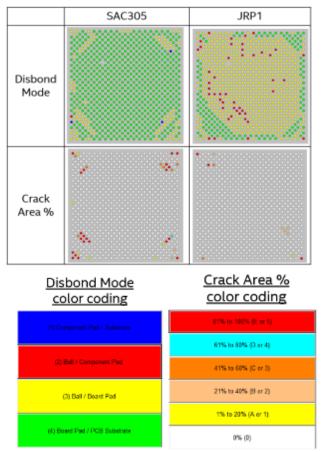


Figure 33. JRP1 end of temp cycle test cross section on both package inner (top) and edge (bottom) rows

Dye and pull FA data, shown in Figure 34, confirmed the failure mode found in the cross section results. The failure mapping of both JRP1 and SAC305 legs showed that the package corners have the most cracks. This result is consistent with the in-situ daisy chain monitoring test data where package corners are the first location to fail on both DOE legs. JRP1 has less number of crack joints when compared to SAC305, highlighting the margin improvement

we saw in temp cycle characteristic life on  $1^{st}$  and  $2^{nd}$  row NCTF DC net.



**Figure 34.** End of Temp Cycle test Dye and Pull crack disbond mode and percentage distribution comparison of SAC305 and JRP1.

### CONCLUSIONS

This study set out to determine the mechanical shock and temperature cycle resistance of mixed SAC-BiSn FCMB BGA solder joints, which were polymerically reinforced by using two Bi-Sn JRPs, JRP1 and JRP2. Their resistance to shock and thermal fatigue was compared with that of SAC solder joints without any reinforcement.

For mechanical shock, results indicated that based on in-situ failures recorded during the shock event, solder joints formed with both JRP1 and JRP2 showed lower number of drops to 63.2% failure when compared to SAC305. CTF failures were seen on both JRP legs, but not on SAC or SAC + Corner fill legs. This indicated that these mixed SAC+BiSn solder joints with polymeric reinforcement were less shock resistant than the SAC solder joints. Based on observed characteristic life on both NCTF nets and CTF nets, the ranking of the solder pastes according to the shock resistance of the solder joints formed when using them is JRP1 < JRP2 < SAC305 < SAC305 + Corner fill.

For thermal fatigue, as determined under temperature cycling, results indicated that solder joints formed when

using JRP1 showed significantly improved temperature cycle performance on the solder joints at the package corners, but for solder joints on inner rows of the package there was not significant difference when compared to that of the SAC solder paste leg. Based on observed characteristic life on 1st and 2nd row corner NCTF and the POP DC package inner net, Temp cycle resistance: JRP1 >> SAC305 on corner most NCTF; JRP1  $\approx$  SAC305 on F26 POP DC net, the ranking of the solder pastes, according to their resistance to thermal fatigue under temperature cycling is: JRP1 >> SAC305 on F26 POP DC net.

From these results, the conclusion that can be surmised is that, although this resin reinforced solution has shown shock performance improvement from mixed SAC+BiSnAg solder joints formed when using traditional BSA solder pastes [3], the two JRP pastes in this study do not show comparable performance to SAC305 paste when subjected to test condition in accordance to JESD22-B111 standard to assess mobile product drop capabilities. Though there was significant improvement in the thermal fatigue resistance of the solder joints formed with one of the JRP pastes evaluated, this improvement was not consistent across all solder joints in the FCMB package array. The encapsulation levels of the solder joints with the reinforcing resin varied widely across the package solder joint array, and this could be one reason for this inconsistency in thermal fatigue improvement. Hence, further work is necessary to understand the effect of resin coverage of solder joints on their temperature cycle performance needs to be better understood.

### **ACKNOWLEDGEMENTS**

The authors would like to acknowledge Russ Brown, Kit Wang, Weiwei Zhou for their contributions and support to SMT, testing, and failure analysis shared in this paper. The authors would also like to acknowledge their management for the valuable guidance and inputs during the course of this year long work, without which this would not have been possible.

#### REFERENCES

- R. Aspandiar, K. Byrd, Kok Kwan Tang, L. Campbell and S. Mokler "Investigation of Low Temperature Solders to Reduce Reflow Temperature, Improve SMT Yields and Realize Energy Savings", <u>Proceedings of the</u> <u>2015 APEX Conference</u>, February 2015.
- 2] S.Mokler, R.Aspandiar, K. Byrd, O.Chen, S.Walwadkar, K.K. Tang, M. Renavikar and S.Sane, "The Application of Bi-based solders for Low Temperature Reflow to Reduce Cost, while Improving SMT Yields in Client Computer Systems", to be published in <u>Proceedings of the 2016 SMTA International Conference</u>, 2016, Chicago, IL.
- 3] M. Holtzer and T. W. Mok, "Eliminating Wave Soldering with Low Melting Point Solder Paste", <u>Proceedings of the 2013 SMTA International</u> <u>Conference</u>, October, 2013.

- 4] M. Holtzer, "Low Temperature SMT Process Conditions", <u>Proceedings of the 2013 IPC APEX</u> <u>Conference</u>, 2013, San Diego, CA
- 5] D. Amir, R. Aspandiar, S. Buttars, W. W. Chin, and P. Gill, "Head-on-Pillow SMT failure Modes", <u>Proceedings of SMTA International Conference</u>, 2009.
- 6] L.Kondrachova, S. Aravamudhan, R. Sidhu, D. Amir, and R. Aspandiar, "Fundamentals of the Non-Wet Open BGA Solder Joint Defect Formation", <u>Proceedings of</u> <u>the International Conference on Soldering and</u> <u>Reliability (ICSR)</u>, 2012.
- 7] Amir, S. Walwadkar, S. Aravamudhan, and L. May, "The Challenges of Non Wet Open BGA Solder Defect", <u>Proceedings of SMTA International</u> <u>Conference</u>, 2012.
- 8] U. Kattner, "Phase Diagrams for Lead-free Alloys, <u>JOM</u>, Volume 54, Issue 12, pp 45-51, Dec 2012.
- 9] Dan Ye, Chengchao Du, Mingfang Wu, Zhongmin Lai, "Microstructure and mechanical properties of Sn-xBi solder alloy", <u>J Mater Sci: Mater Electron (2015)</u> Vol 26, pp 3629–3637.
- 10] J. Glazer, "Microstructure and Mechanical Properties of Lead-free alloys for low cost electronics assembly", <u>Journal of Electronic Materials</u>, Vol 23, 8, (1994), pp 693-700.
- 11] V. A. Skudnov, L. D. Sokolov, A. N. Gladkikh, V. M. Solenov, "Mechanical properties of bismuth at different temperature and strain rates", <u>Metal Science and Heat</u> <u>Treatment</u>, December 1969, Vol 11, pp 981–984.
- William D. McCallister, <u>Material Science and Engineering: An Introduction</u>, 6<sup>th</sup> edition, John Wiley & Sons, 2003, pg 168.
- 13] Ranjit Pandher and Robert Healey, "Reliability of Pb-Free Solder Alloys in Demanding BGA and CSP Applications", <u>Proceedings of the IEEE 58th Electronic</u> <u>Components and Technology Conference (ECTC)</u>, 2008.
- 14] Yan Liu, Joanna Keck, Erin Page, and Ning-Cheng Lee, "Voiding And Reliability of BGA Assemblies with SAC and 57Bi42Sn1Ag Alloys", <u>Proceedings of the</u> <u>SMTA International Conference</u>, 2013.
- 15] Yan Liu, Joanna Keck, Erin Page, and Ning-Cheng Lee, "Voiding And Drop Test Performance of Lead-free Low Melting and Medium Melting Mixed Alloy BGA Assembly,, <u>Proceedings of the IPC APEX</u> <u>Conference</u>,2014.
- 16] Olivia H Chen, Kevin Byrd, Scott Mokler, Kok Kwan Tang, and Raiyo Aspandiar, "Comparison Of The Mechanical Shock/Drop Reliability Of Flip Chip BGA (FCBGA) Solder Joints Formed By Soldering With Low Temperature BiSn-Based Resin Reinforced Solder Pastes", <u>Proceedings of the International Conference on Soldering and Reliability (ICSR)</u>, 2015.
- 17] O.H. Chen, A. Molina, R. Aspandiar, K.Byrd, S.Mokler and K.K. Tang, "Mechanical Shock and Drop Reliability Evaluation of the BGA Solder Joint Stank-Ups formed by Reflow Soldering SAC Solder Ball BGAs with BiSnAg and Resin-Reinforced Solder

Pastes", <u>Proceedings of SMTA International</u> <u>Conference</u>, 2015, Rosemont, IL.

- [18] JESD22-B111, "Board Level Drop Test Methods for Handheld Electronics", JEDEC, 2003
- 19] IPC-9701A, "Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments," <u>IPC</u>, February 2006.